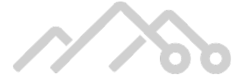
PCB 101 – How Boards are Manufactured

Summit Interconnect's Proprietary Information

Presenter



Laura Martin

Director of Applications Engineering – Summit Interconnect

Laura Martin specializes in PCB Design for Manufacturing and works with customers to promote best design practices for manufacturability based on industry standards and Summit's technical capabilities.

Laura previously worked for Lockheed Martin for 15 years, initially in PCB manufacturing and then as leader of the producibility engineering department where she and her team reviewed all circuit board designs prior to release for manufacturing.

Email:
Laura.Martin@SummitInterconnect.com

Phone: (407) 212-8652

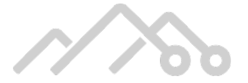
Overview

Summit is the largest privately held PCB manufacturer in North America

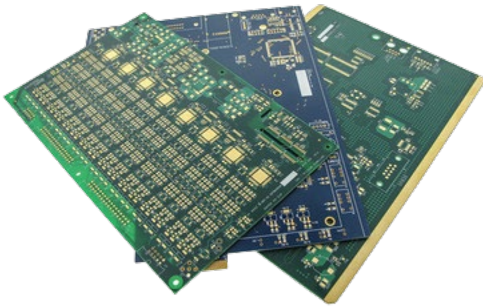
- Eight North American-based facilities
- Multiple sites provide redundancy for customer risk mitigation
- Focused on providing the best customer experience with easy ordering and full transparency
- Broad range of PCB product capabilities
- Extensive quality certifications with continuous improvement processes

A total PCB solution from quick-turn prototype to volume production in a single manufacturing partner

A Complete Portfolio of PCB Products

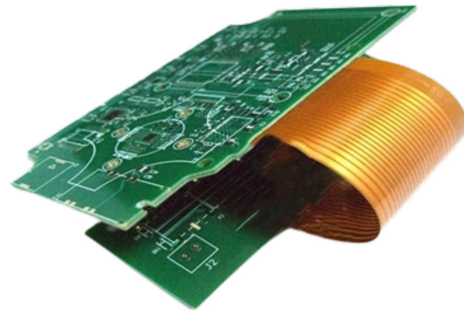


Rigid



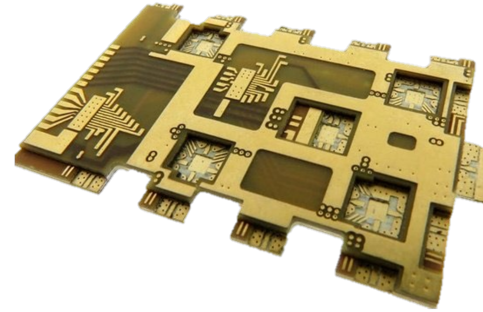
- High layer count
- Stacked microvias
- Complex miniature structures (i.e. blind/buried vias, via fill)
- Back drilling
- Multiple sequential lam
- Heat sinks
- Bonded, embedded coins
- Same-day turns available

Flex, Rigid-Flex



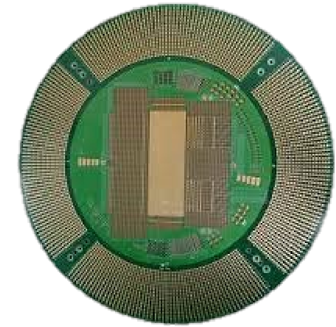
- Oversize, loose-leaf, bookbinder constructions
- Single-sided, double-sided, and multi-layer flex
- Adhesiveless and adhesive
- Stiffeners and connectors
- Laser ablation
- Thin flex laminates
- Flex assembly

RF / Microwave



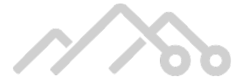
- RF/digital hybrid designs
- Wide range of PTFE materials
- Mixed material stackups
- Plated cavities, edge plating
- Mode suppression/stitching
- Buried resistors
- Edge launch features

Semiconductor/ATE



- Reference, probe and load, and burn-in-boards
- High aspect ratio
- Low loss materials
- Bondable gold
- Tight tolerance drilling
- Ormet bonding
- Oversized panel options

PCB Fabrication Process



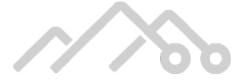
Receive Customer Files → 1 Front-End Engineering → 2 Issue & Prep Material → 3 Inner Layer Image & Develop → 4 Inner Layer Etch & Strip → 5 Inner Layer Lamination

→ 6 Drill → 7 Plasma, Desmear, Etchback → 8 Electroless Copper Plate → 9 Outer Layer Image & Develop → 10 Electrolytic Copper Plate → 11 Electrolytic Tin Plate

→ 12 Outer Layer Strip & Etch → 13 Strip Tin Plating → 14 Solder Mask → 15 Final Finish → 16 Ink Legend → 17 Electrical Test

→ 18 Route Boards & Coupons → 19 Final Inspection → 20 Coupon Microsection & Analysis → Package & Ship Boards

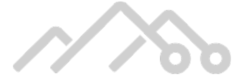
Step 1: Front-End Engineering



The process of **converting** customer **design** files to **working** data.

- Planning Steps
  - Review of all documentation
  - Select material and panel size
  - Create material stack up and calculate impedance (if required)
  - Create manufacturing travelers
  - Release order to manufacturing floor
- CAM Steps
  - Import customer data
  - Perform net compare & DFM checks
  - Prepare data for manufacturing
  - Panelize 1-up board
  - Output files to production equipment

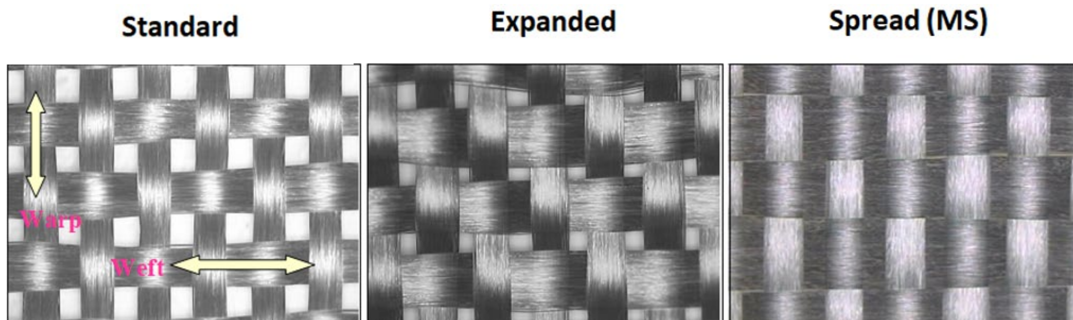
Base Materials



Rigid Material

IPC-4101 & IPC-4103

- Laminate Cores – cured resin and glass fabric with copper on each side
- Prepreg Sheets – uncured resin and glass fabric with no copper
- Different IPC slash sheets have different material properties

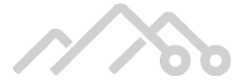


Copper Foil

IPC-4562

- Weight
  - 1/4 oz, 3/8 oz, 1/2 oz, 1 oz, etc.
- Types
  - Reverse Treated Foil (RTF)
  - Very Low Profile (VLP)
  - Rolled Annealed (RA)
  - Etc.

Step 1: Front-End Engineering - Planning



Fabrication Stackup

Lyr	s-p	Layer Type	FThick **	PThick	MClad	FClad	qty	Core/PP	CC	Base	Foil	System	Fill Loss	Cu. %	Ω	dK
1	m		0.0021		0.50	1.50					F	0.0021		100.00		
			0.0037	0.0047			1	MW2211655		MW2		0.0037	0.0011			
2	m		0.0021		0.50	1.50					F	0.0021		50.00		
			0.0023	0.0024			1	MW2106 77		MW2		0.0023	0.0001			
3	m		0.0044		0.50	0.50		0.0030		MW2	F	0.0044		85.00		
4	m				0.50	0.50					F			90.00		
			0.0023	0.0024			1	MW2106 77		MW2		0.0023	0.0001			
5	m		0.0044		0.50	0.50		0.0030		MW2	F	0.0044		90.00		
6	p				0.50	0.50					F			85.00		
			0.0042	0.0047			1	MW2211655		MW2		0.0042	0.0005			
7	m		0.0094		0.50	0.50		0.0080		MW2	F	0.0094		50.00		
8	p				0.50	0.50					F			85.00		
			0.0042	0.0047			1	MW2211655		MW2		0.0042	0.0005			
9	m		0.0094		0.50	0.50		0.0080		MW2	F	0.0094		50.00		
10	p				0.50	0.50					F			90.00		
			0.0023	0.0024			1	MW2106 77		MW2		0.0023	0.0001			
11	m		0.0044		0.50	0.50		0.0030		MW2	F	0.0044		90.00		
12																
13																
14																
15																
16																

IPC Slash Sheet

SPECIFICATION SHEET

Specification Sheet #: IPC-4101/41
Reinforcement: *1:* Woven E-glass — *2:* NONE
Resin System: *Primary:* Polyimide; *Secondary 1:* NONE — *Secondary 2:* NONE
Flame Retardant Mechanism: AABUS — *Minimum UL94 Requirement:* HB
Fillers: With or without inorganic fillers
ID Reference: *UL/ANSI:* GPY; *ANSI:* GPY/41 — *MIL-S-13949:* /10 - GIL, GIP
Glass Transition (T_g): 250 °C minimum

LAMINATE REQUIREMENTS

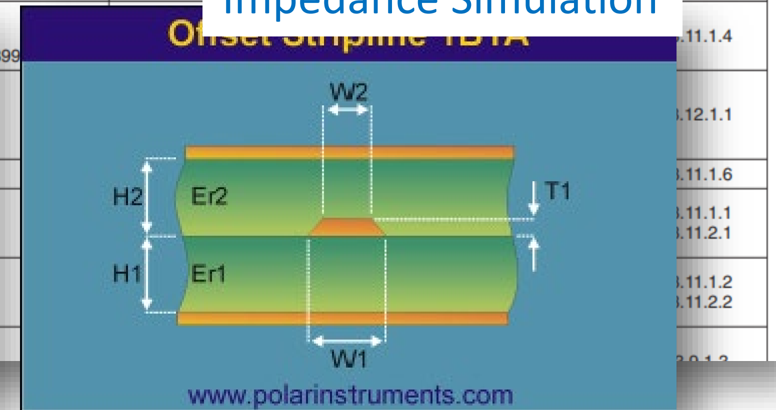
Laminate Requirement	Specification <0.50 mm [0.0197 in]	Specification ≥0.50 mm [0.0197 in]	Units	Test Method	Ref. Para.
1. Peel Strength, minimum					3.9.1.1
A. Low profile copper foil and very low profile copper foil – all copper foil >17 µm [0.669 mil].	AABUS	AABUS	N/mm [lb/in]	2.4.8	
B. Standard profile copper foil				2.4.8.2	
1. After thermal stress	0.70 [4.00]	0.80 [4.57]		2.4.8.3	3.9.1.1.1
2. At 125 °C [257 °F]	0.60 [3.43]	0.70 [4.00]			3.9.1.1.2
3. After process solutions	0.60 [3.43]	0.70 [4.00]			3.9.1.1.3
C. All other foil – composite	–	–			
2. Volume Resistivity, minimum					
A. After humidity conditioning	6 x 10				.11.1.3
B. At elevated temperature (204 °C [399.2 °F])	6 x 10				

Manufacturer's Material Data Sheet

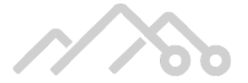
Prepreg Data

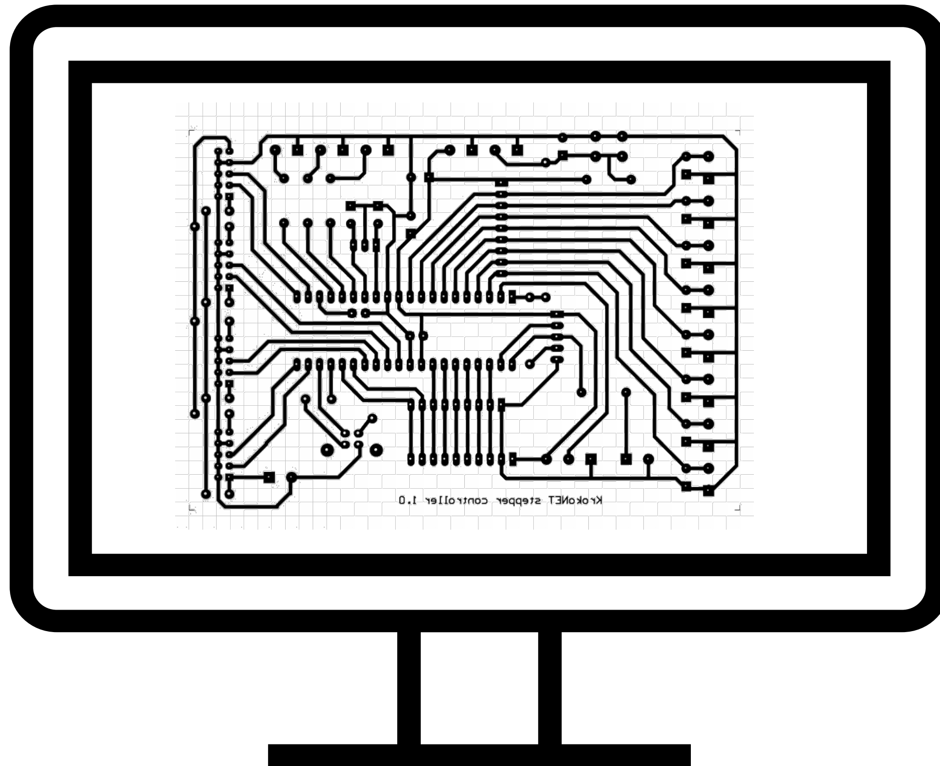
Glass Style	Resin Content %	Thickness (inch)	Thickness (mm)	Dielectric Constant (DK)/ Dissipation Factor (DF)					
				100 MHz	500 MHz	1 GHz	2 GHz	5 GHz	10 Ghz
106	75.00%	0.0024	0.061	3.48 0.0158	3.43 0.0180	3.41 0.0208	3.38 0.0218	3.35 0.0229	3.35 0.0259
1080	65.00%	0.0032	0.081	3.66 0.0146	3.62 0.0165	3.60 0.0189	3.57 0.0198	3.54 0.0207	3.54 0.0233
2113	57.00%	0.004	0.102	3.81	3.78	3.76	3.74	3.71	3.71

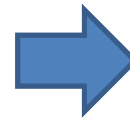
Impedance Simulation

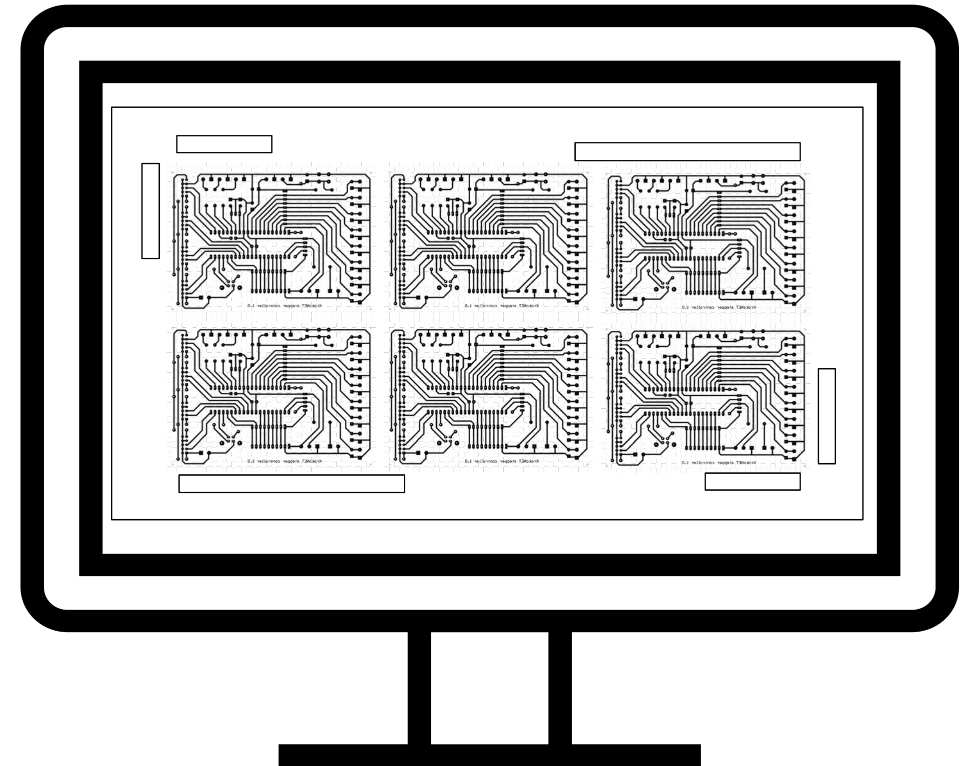


Step 1: Front-End Engineering - CAM





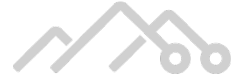




1-up board design

Multiple boards and test coupons placed in an array on selected panel size

Step 2: Issue & Prep Material



- Core laminate is cleaned with an acid dip prior to photoresist process
- Prepreg sheets get tooled for lamination

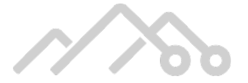
Resin, glass, and copper substrate

a. Rigid core laminate

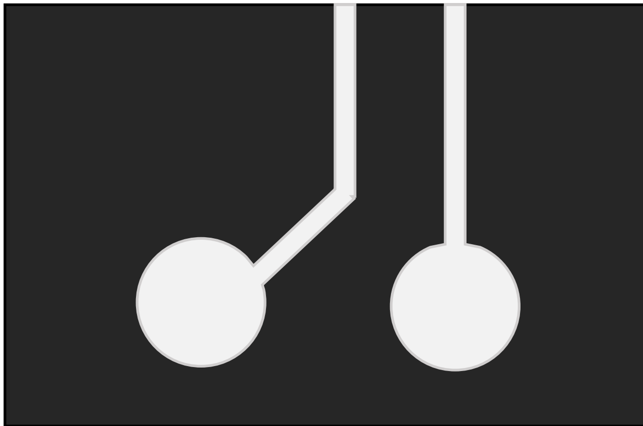
Substrate is coated with photo-imageable resist

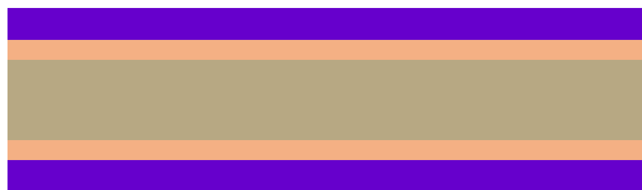
b. Photoresist coat

Step 3: Inner Layer Image & Develop



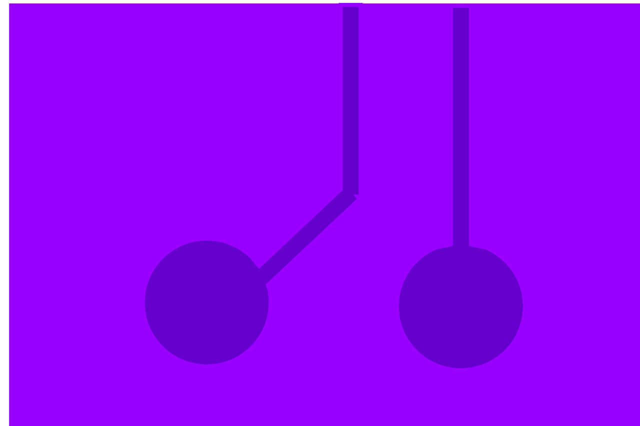
Circuit pattern is transferred to resist coated laminate by LDI

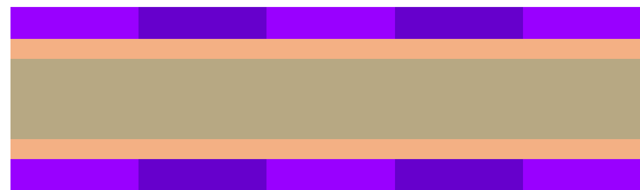




c. Image transfer

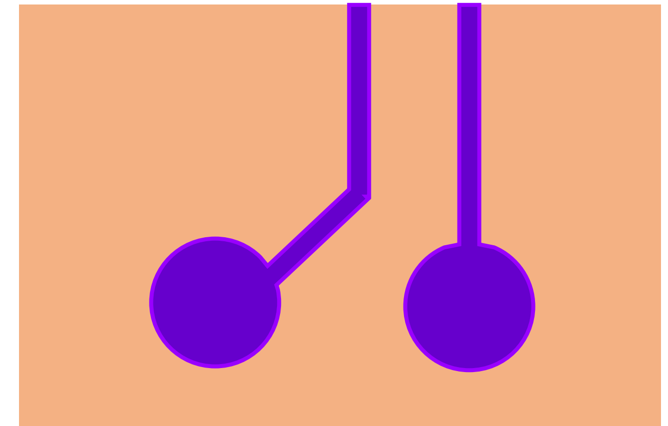
Pattern in resist is cured by the laser in previous step

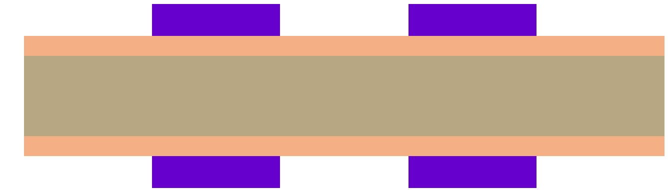




d. Polymerized pattern in resist

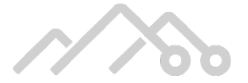
Uncured resist is dissolved away



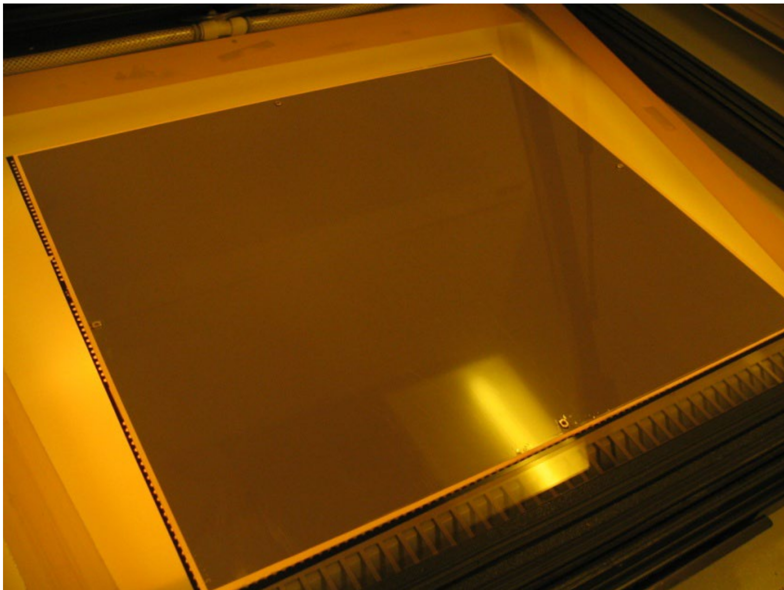


e. Circuit pattern in resist

Laser Direct Image Equipment

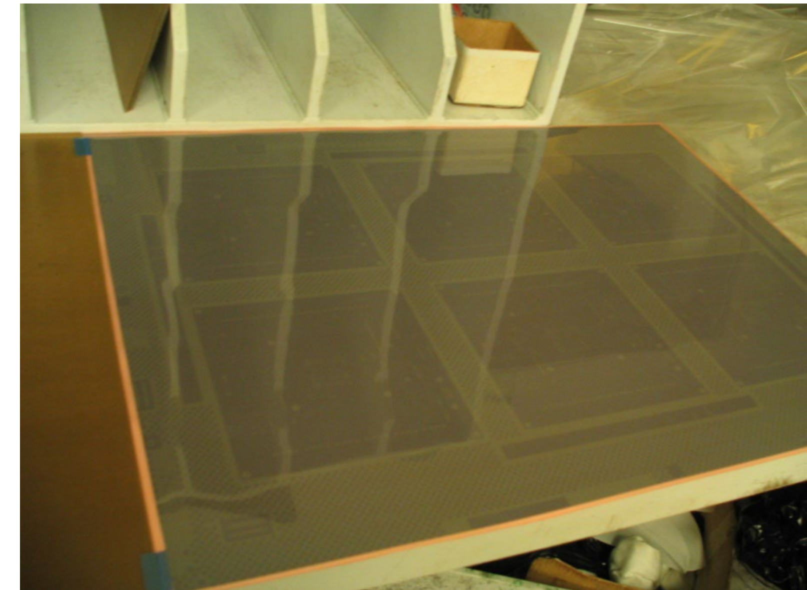


Inner layer coated with resist

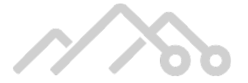


Laser Direct Image Machine

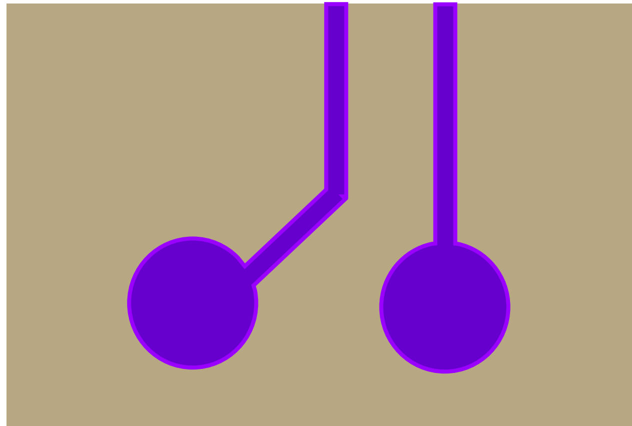
Inner layer image transferred

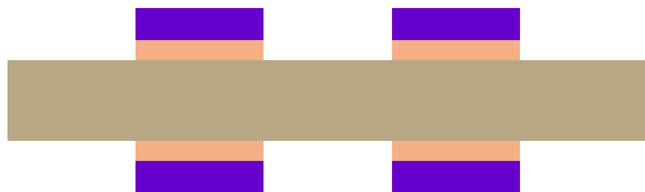


Step 4: Inner Layer Etch & Strip



Exposed copper is etched away down to the substrate





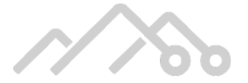
f. Etch copper

Resist is stripped and finished copper pattern remains

g. Final result

- Finished layers then get post-etch punched in preparation for the next process: Inner Layer Lamination

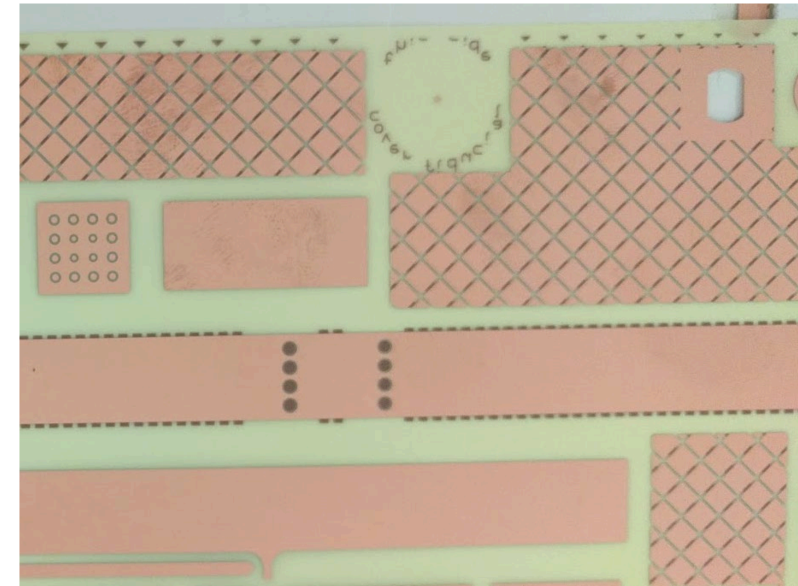
DES Line



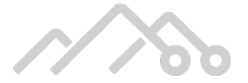
Develop, Etch, Strip (DES) Line

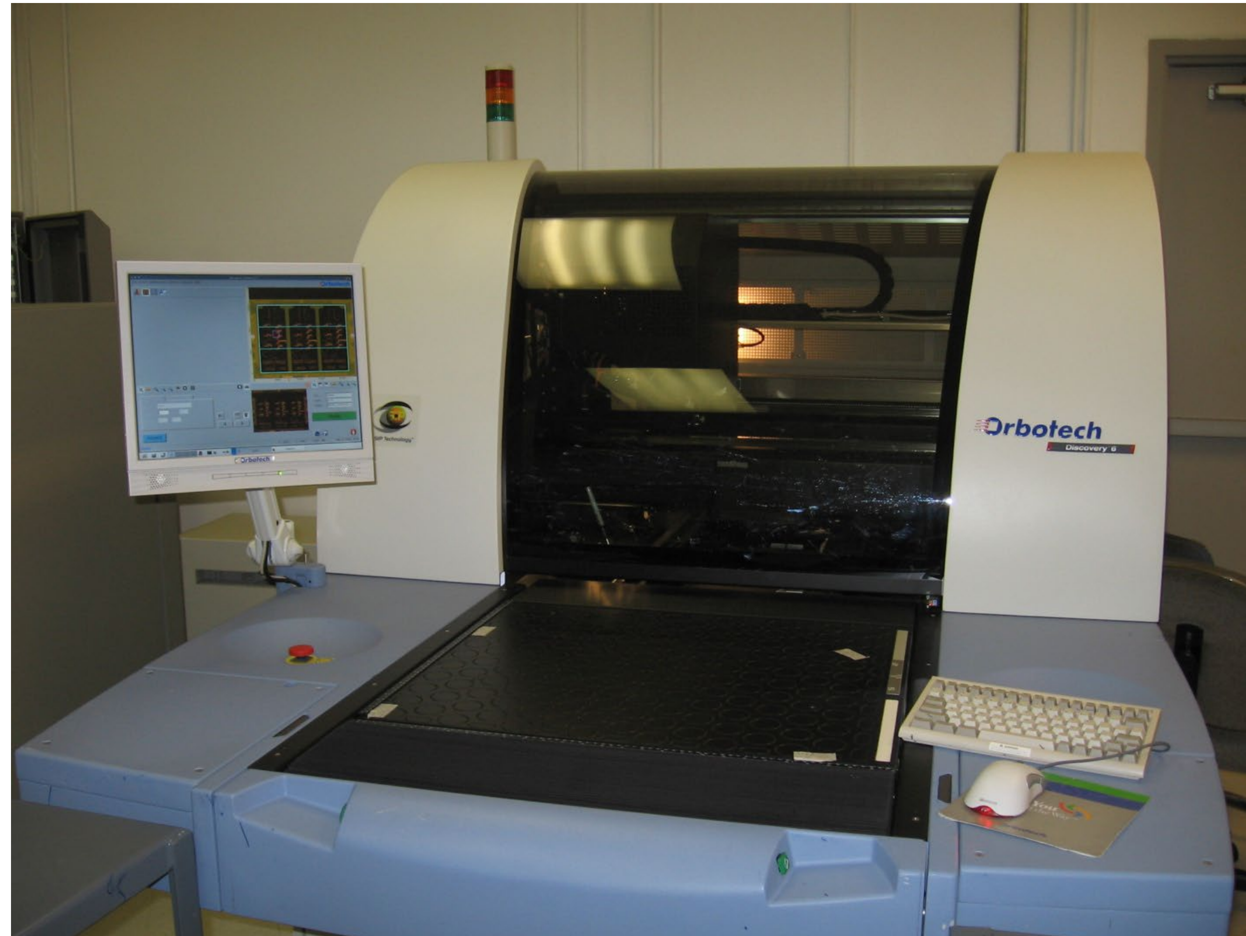
Completed inner layer

Post-etch punch

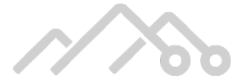


Automated Optical Inspection





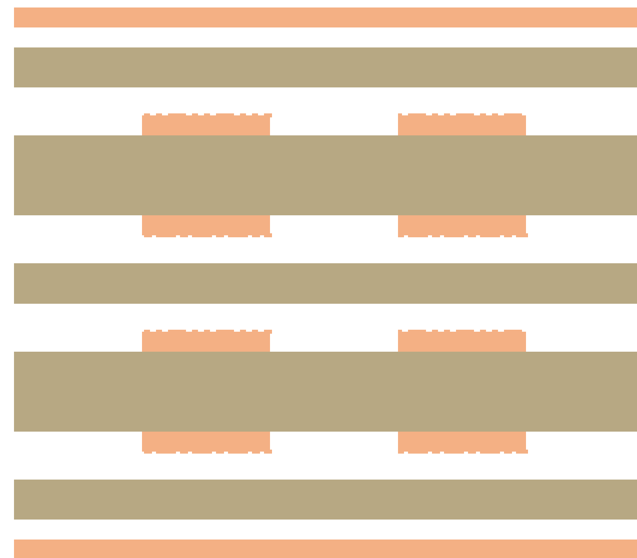
Step 5: Inner Layer Lamination



Copper is roughened (by oxide) to promote adhesion for lamination

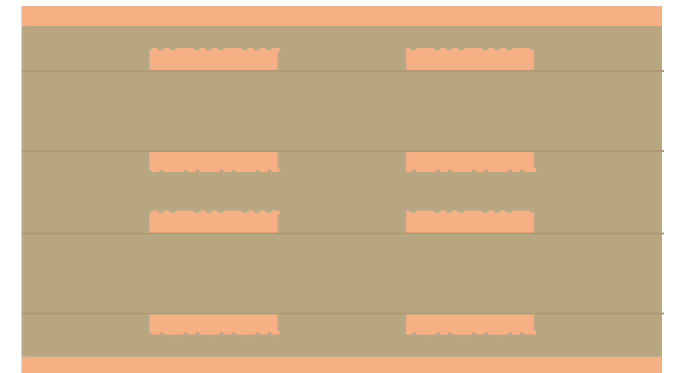
h. Roughened copper

Laminate, prepreg, and outer copper layers are stacked up for lamination



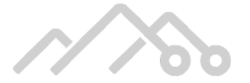
i. Materials stacked up

Final result (often referred to as a sub or panel)

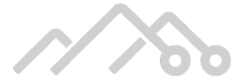


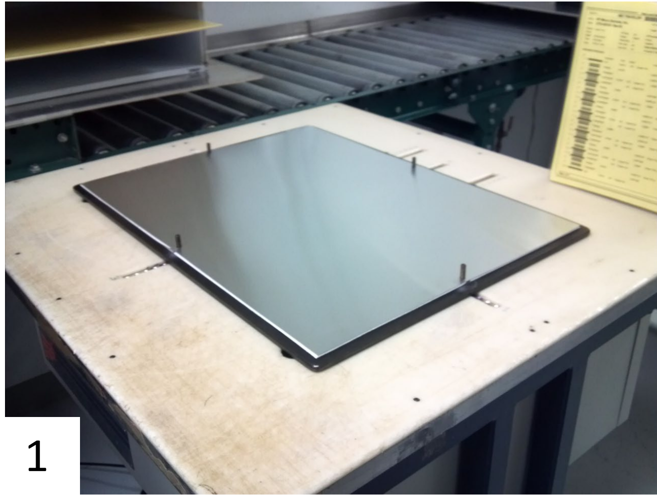
j. Laminated stackup

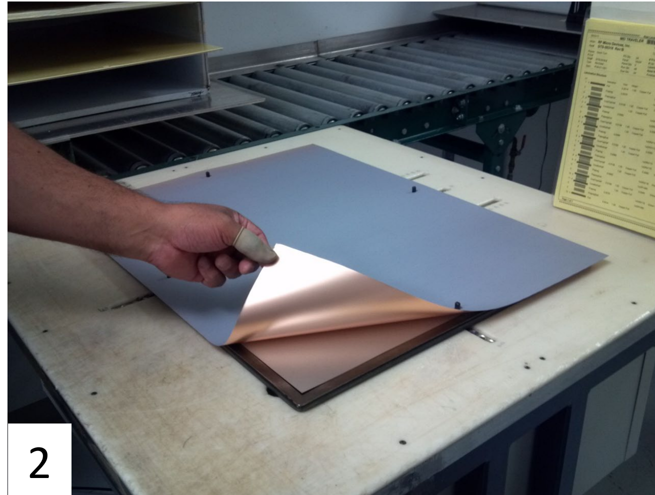
Inner Layer Surface Oxide

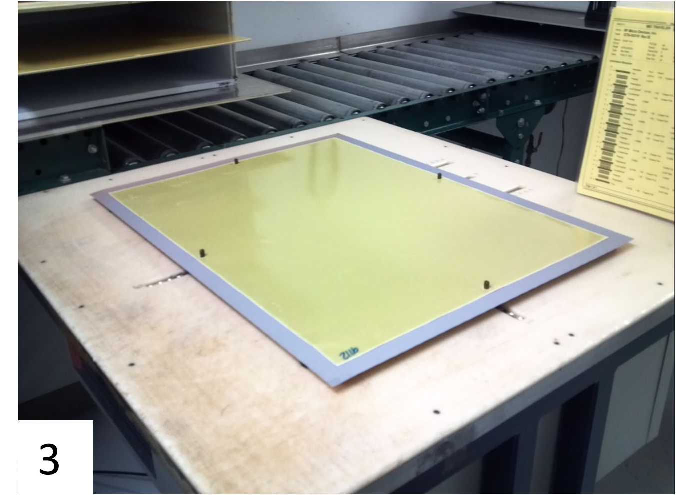


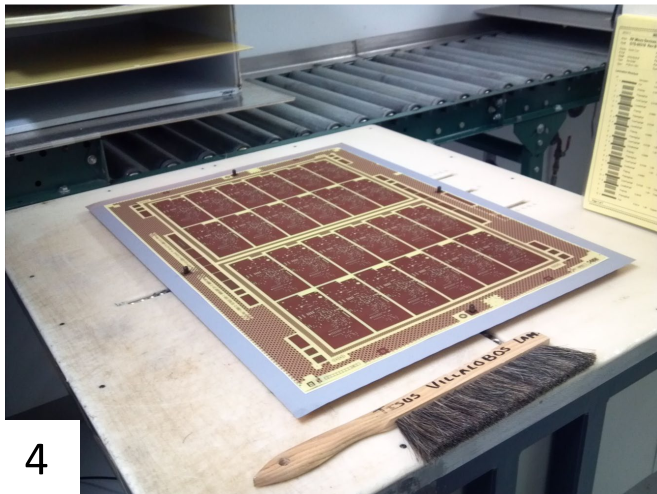
Lamination Layup

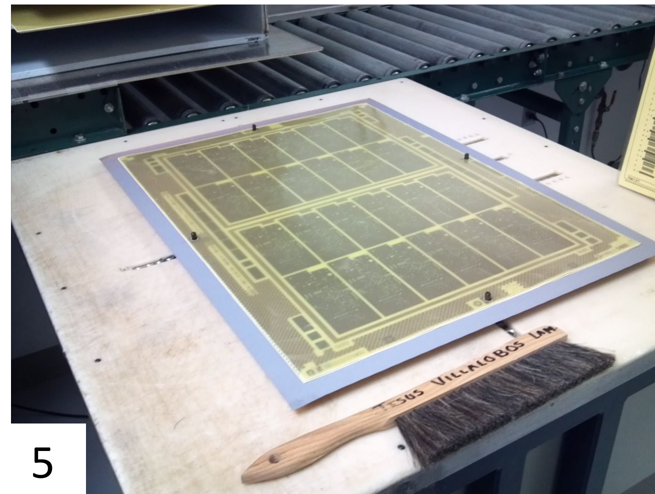




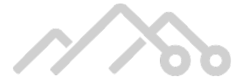




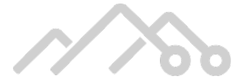




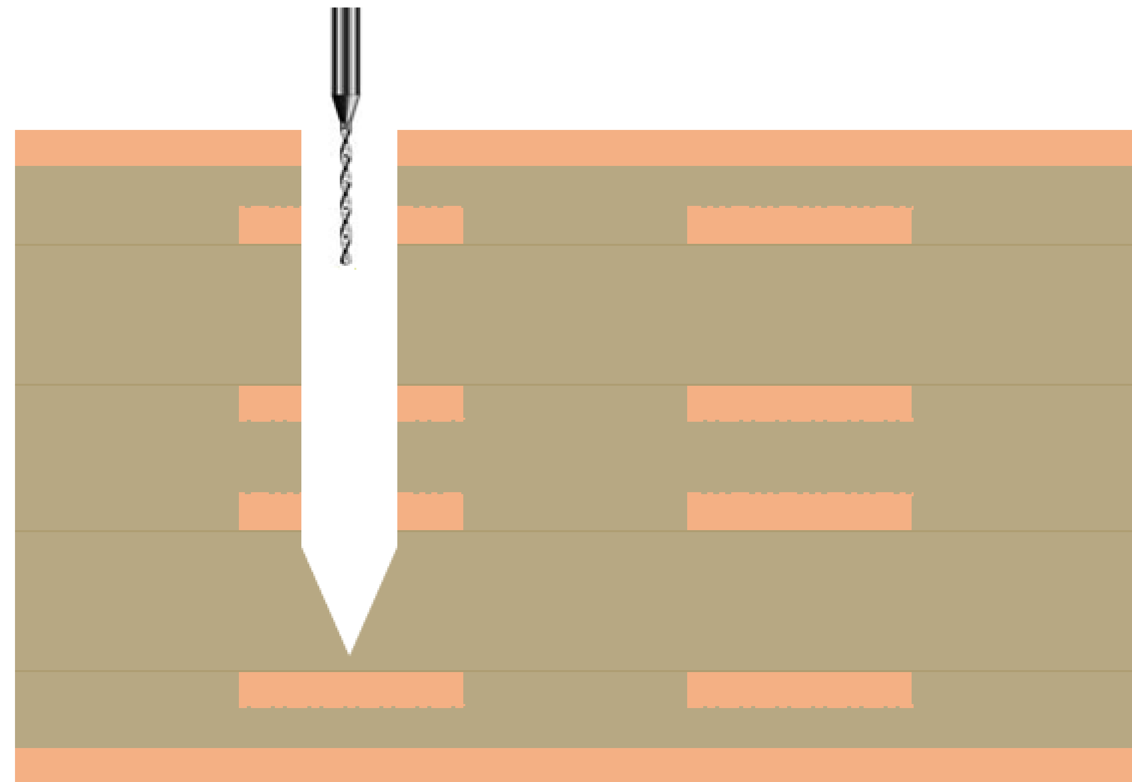
Lamination Press Machine



Step 6: Drill

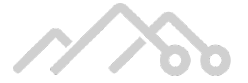


- Prior to drilling, the panel is “flash routed” to remove resin squeeze-out from edges of panel
- An in-process coupon is “test” drilled and x-rayed to check registration prior to entire panel being drilled



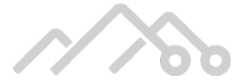
k. Drilling holes in laminated panel

Mechanical Drill



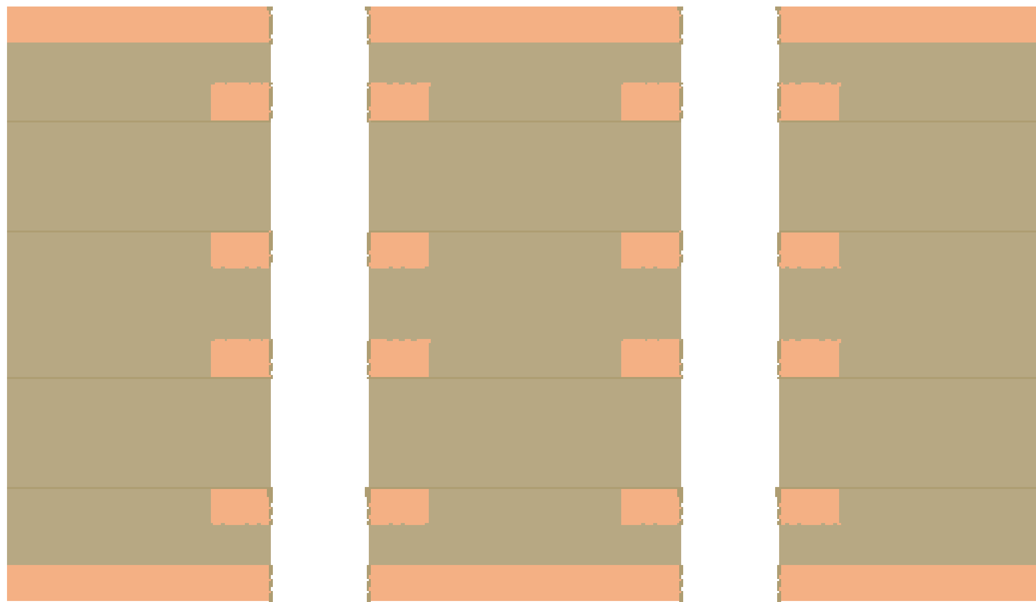
Mechanical Drill

Step 7: Desmear, Plasma, Etchback

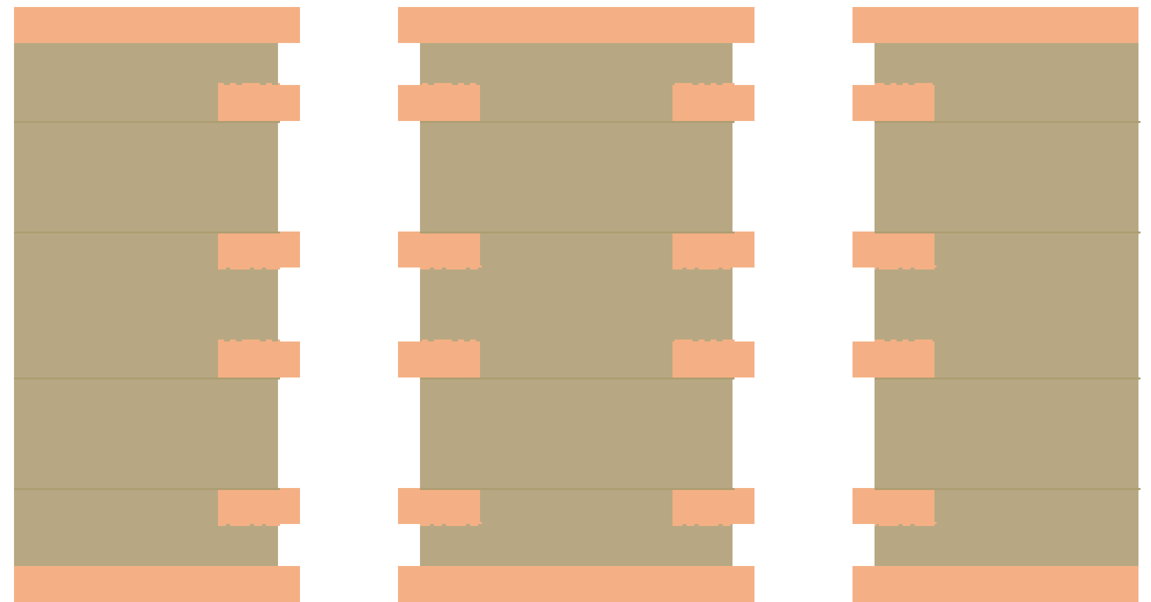


Drilled holes need to be prepared for electroless copper plating

A series of steps is performed to desmear and etch back copper

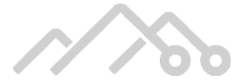


l. Resin smear in holes after drill process



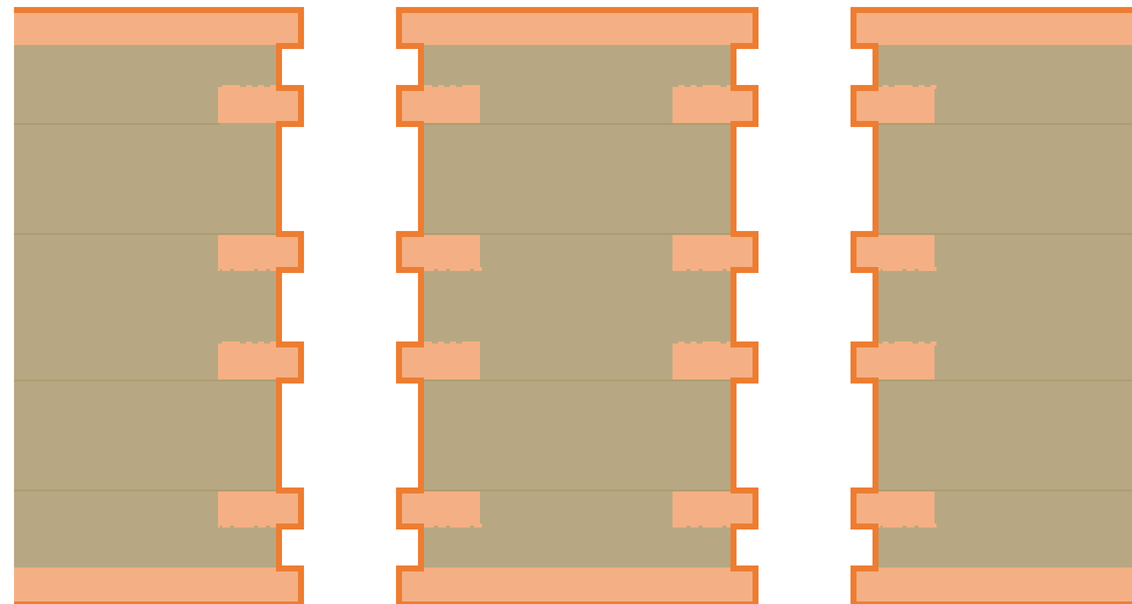
m. Cleaned and prepped holes, and etchback

Step 8: Electroless Copper Plate



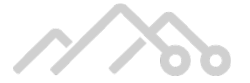
- A conditioner charges side walls
- The palladium is attracted
- The reaction allows copper to start plating

Thin layer of electroless copper is chemically plated on non-conductive material

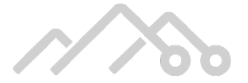


n. Electroless copper deposition

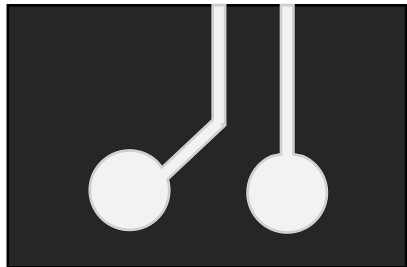
Hole Cleaning and Electroless Line



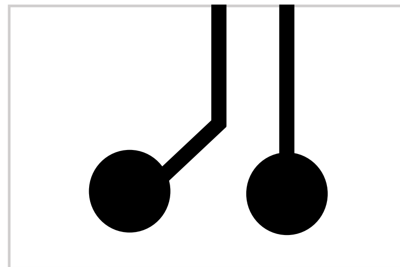
Step 9: Outer Layer Image & Develop



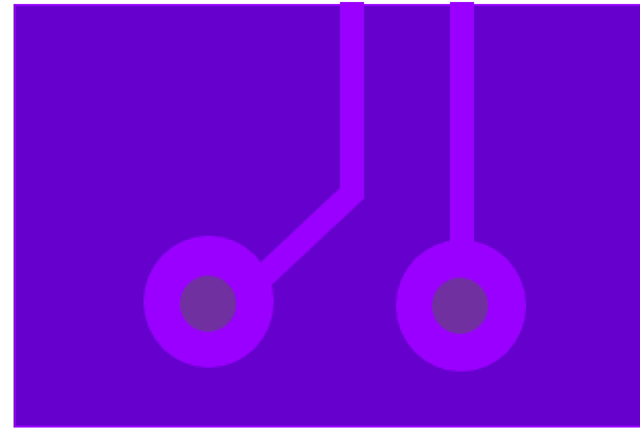
- Same process as inner layers, except the reverse image is polymerized now
- Panel is coated with photoresist and outer layer image is transferred by LDI
- Resist dissolves over pattern to be plated

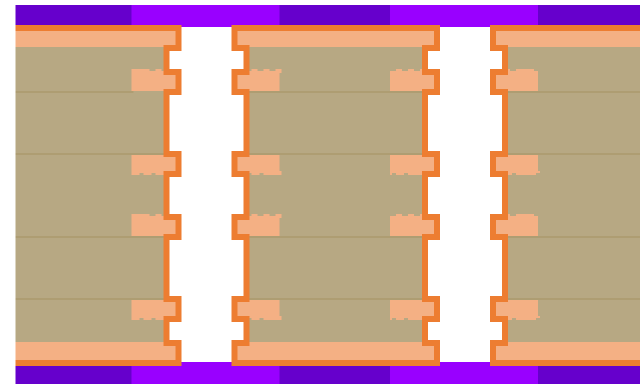


Inner layer image (negative)

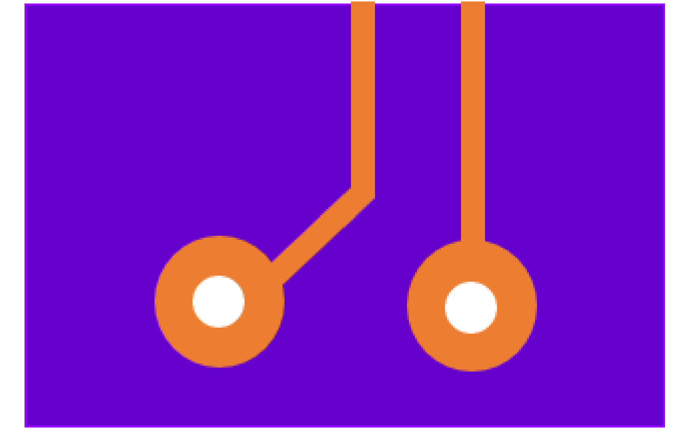


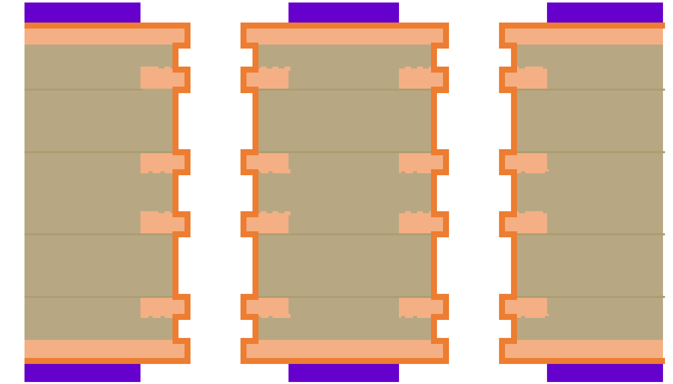
Outer layer image (positive)





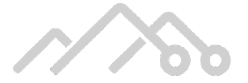
o. Panel coated in photoresist

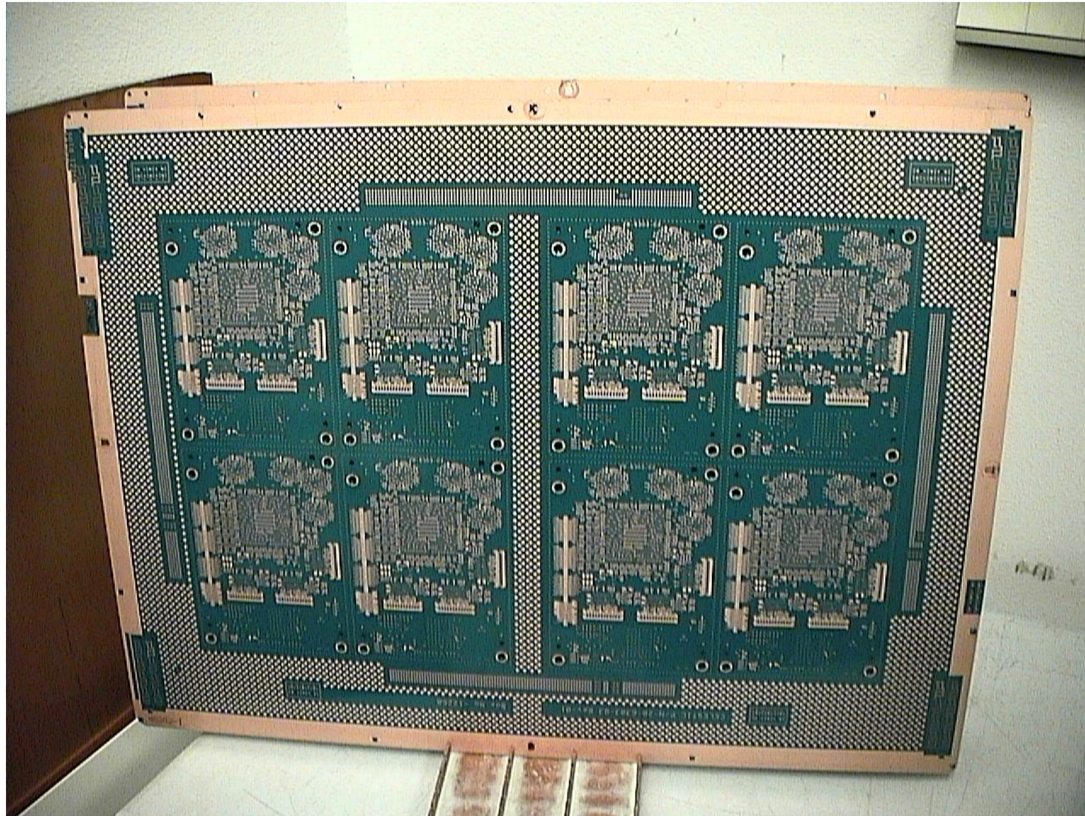


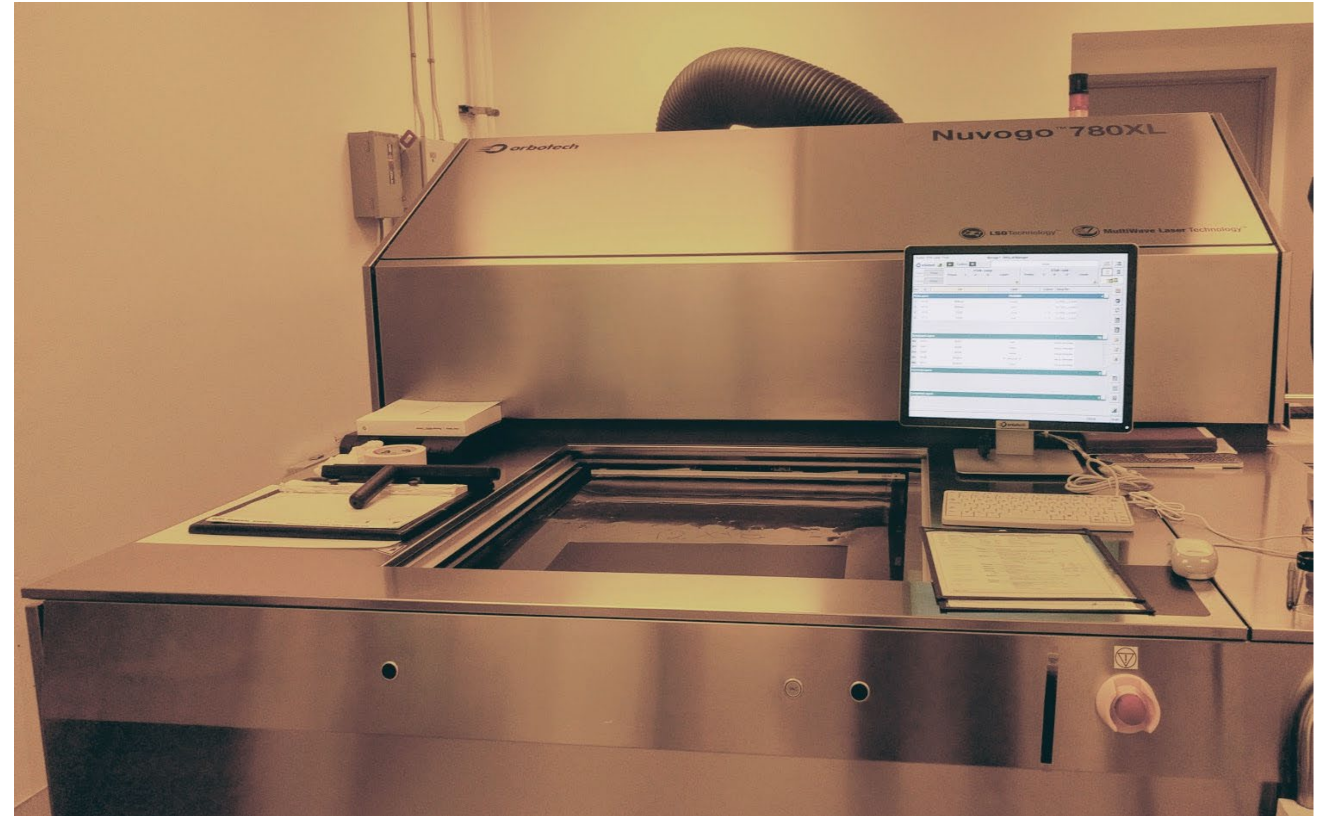


p. Outer layer image transferred

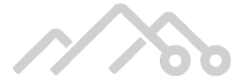
Outer Layer Image





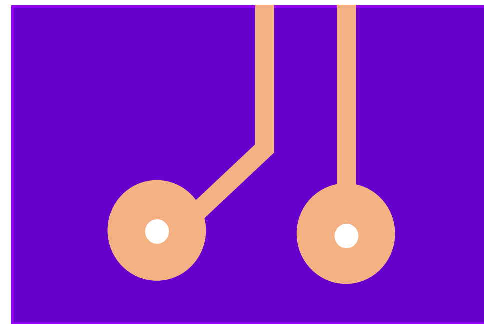


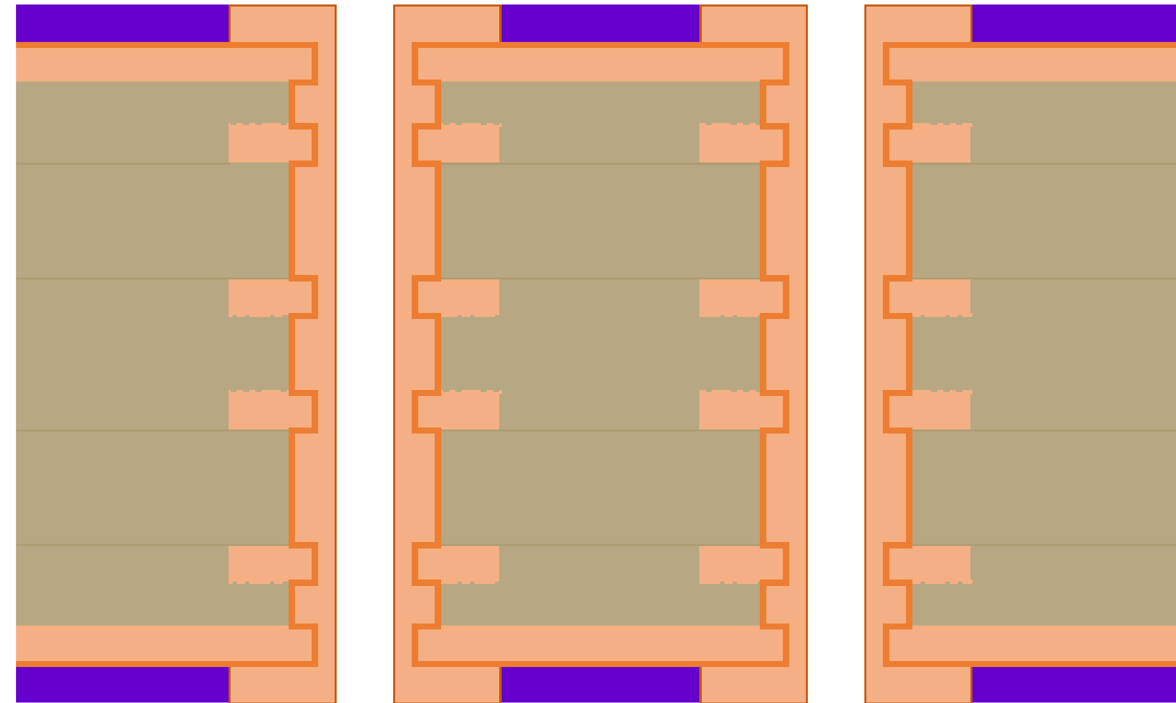
Step 10: Electrolytic Copper Plate



- Electricity can now be used to plate surfaces made conductive from the electroless plating step

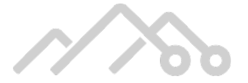
Copper is electrically plated until hole wall thickness requirements are met



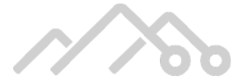


q. Resist-free area is plated with electrolytic copper

Electrolytic Plating Line

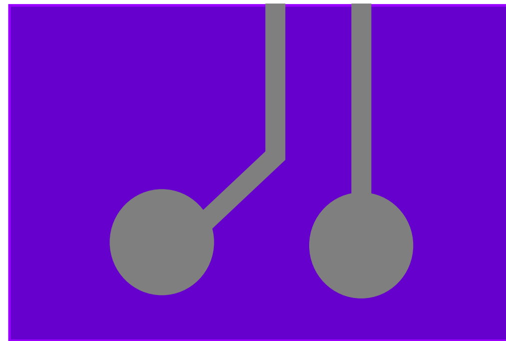


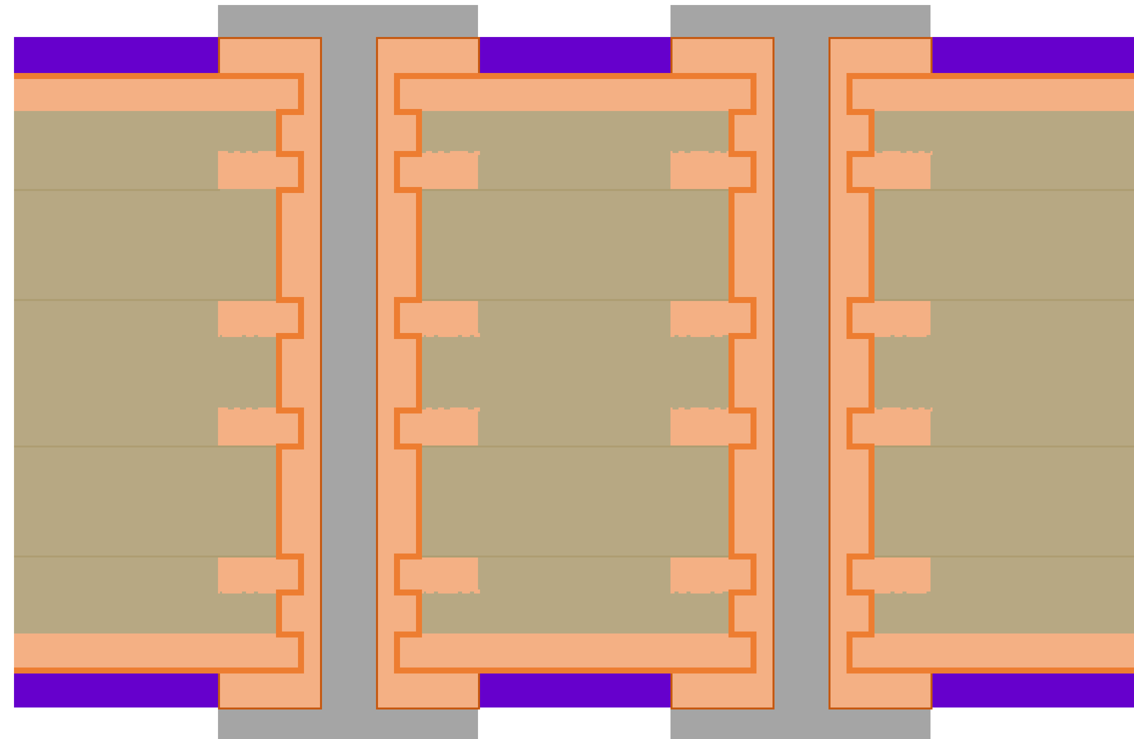
Step 11: Electrolytic Tin Plate



- Similar to photoresist, the plated tin protects the copper and can withstand the resist strip chemicals

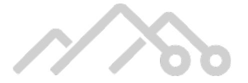
Tin is plated over exposed copper and acts as a resist for the next process



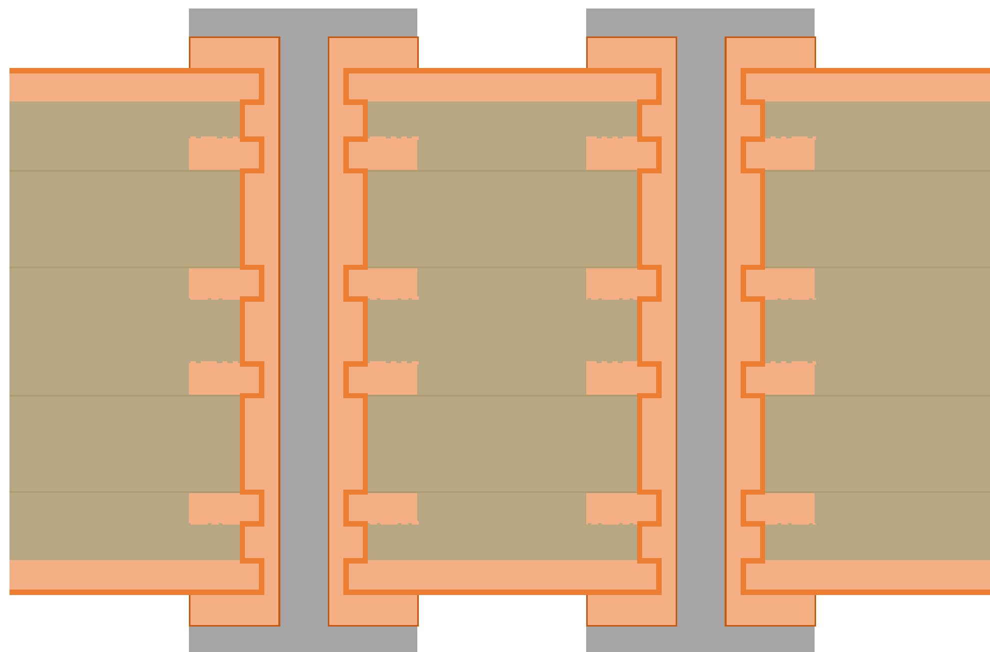


r. Tin “resist” plating

Step 12: Outer Layer Strip & Etch

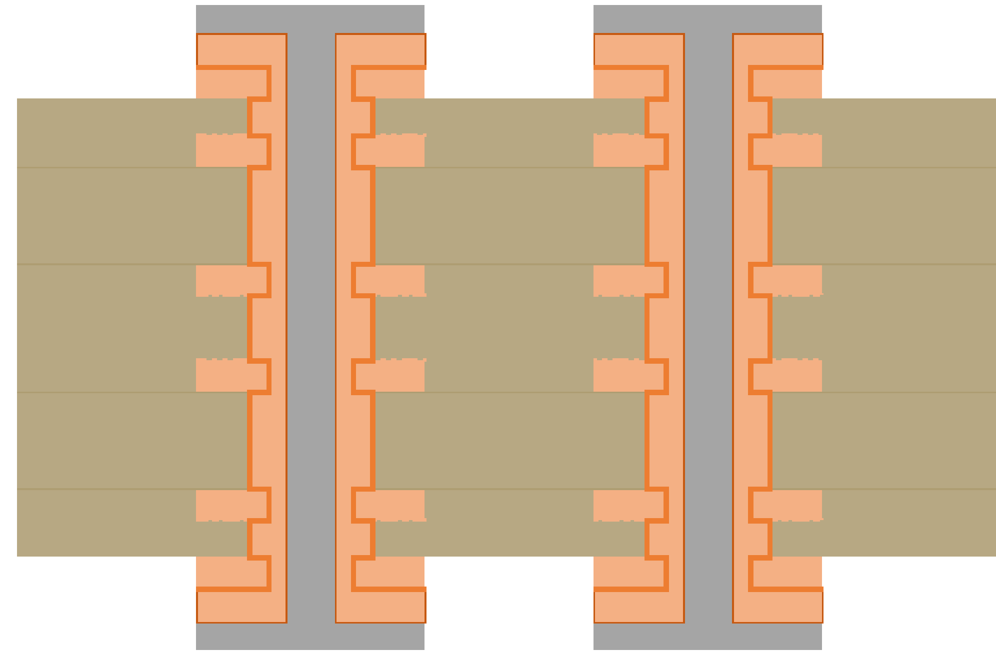


The photoresist is stripped away, and remaining copper is exposed



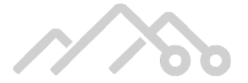
s. Stripped resist

Remaining exposed copper is etched away down to substrate

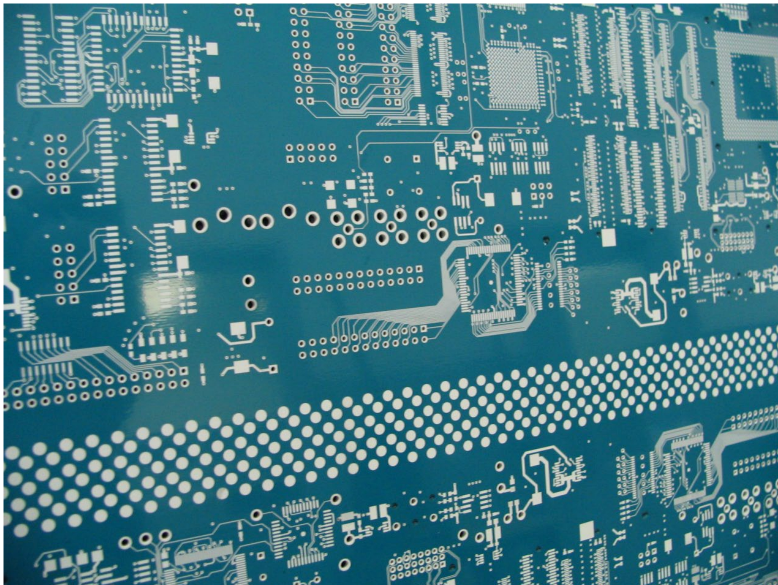


t. Etched copper

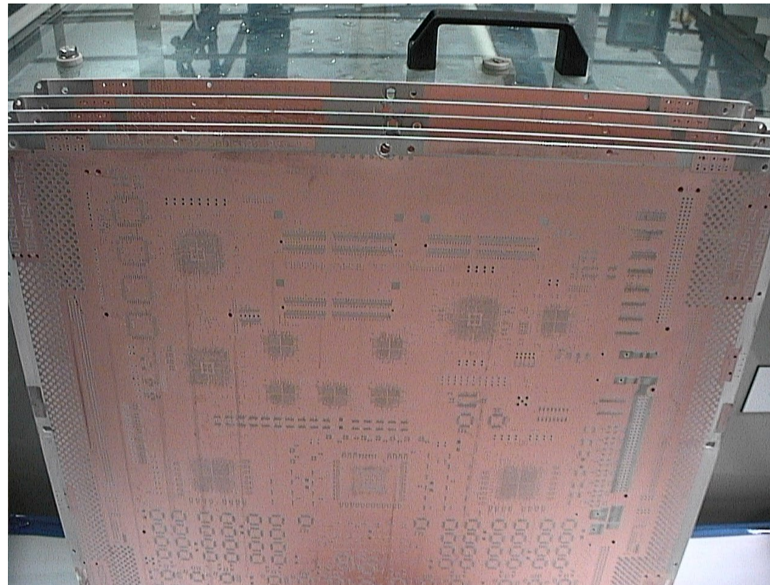
Tin Plate, Strip, and Etch



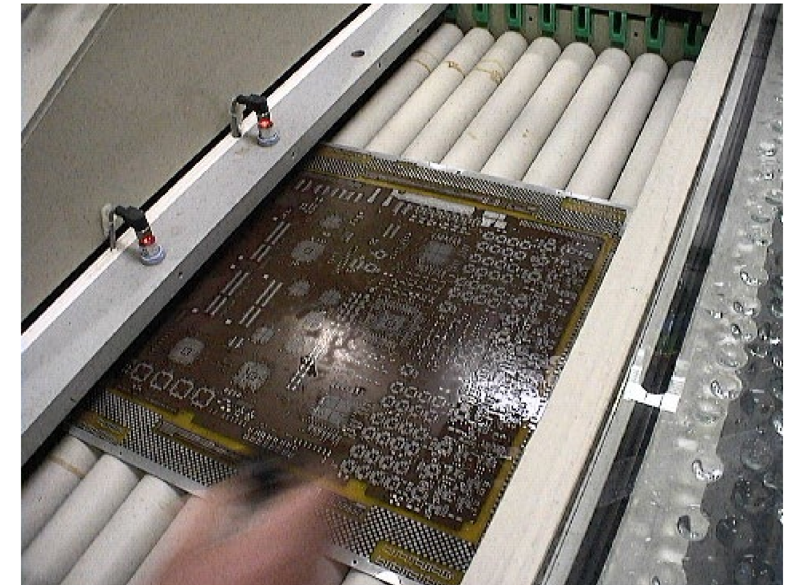
Tin plate with resist



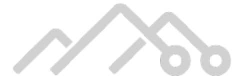
Resist stripped



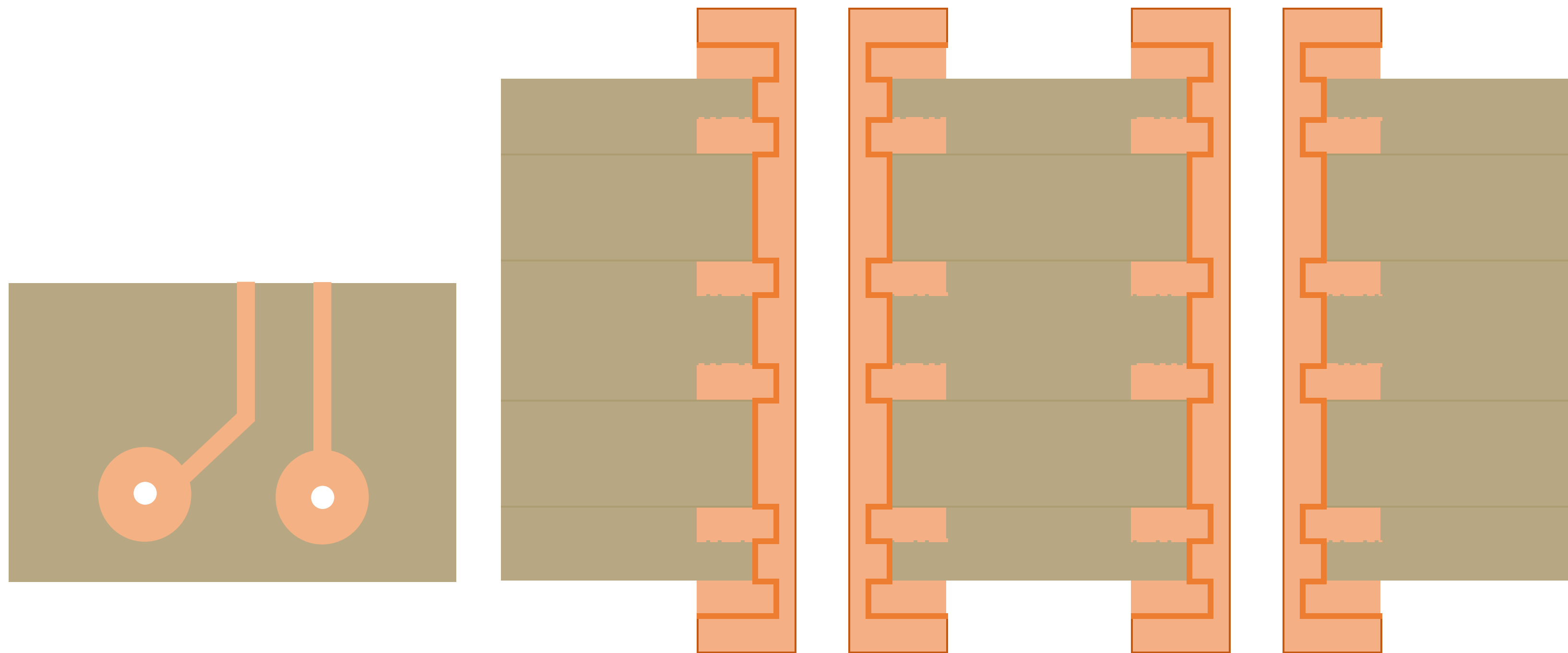
Etched copper



Step 13: Strip Tin Plating

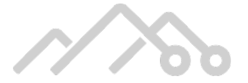


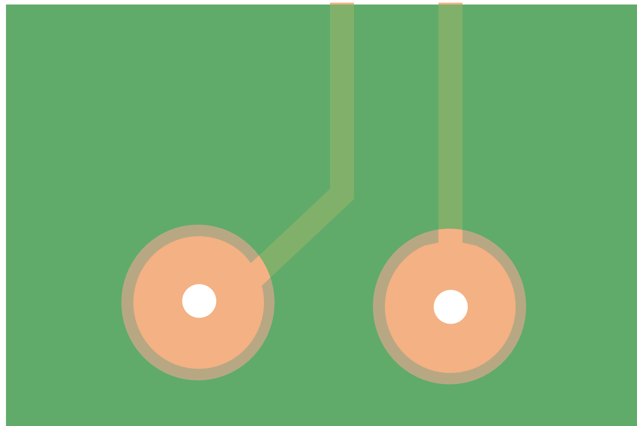
Tin “resist” is stripped from panel, revealing final circuit pattern

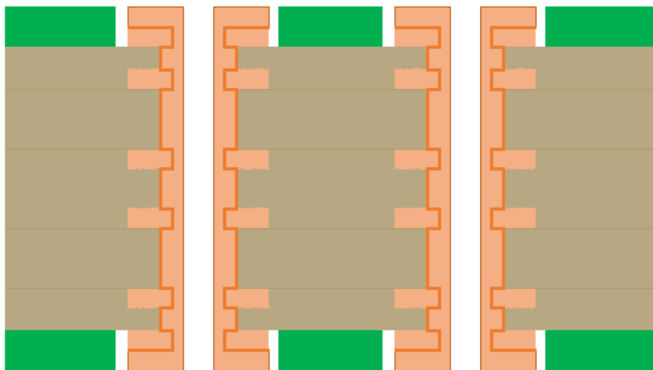


u. Final step of outer layer image transfer

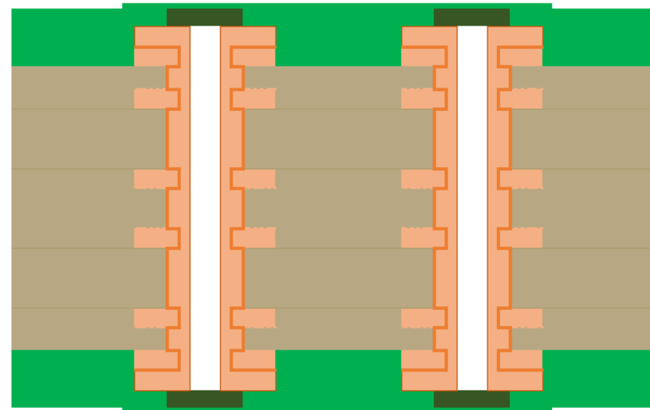
Step 14: Solder Mask



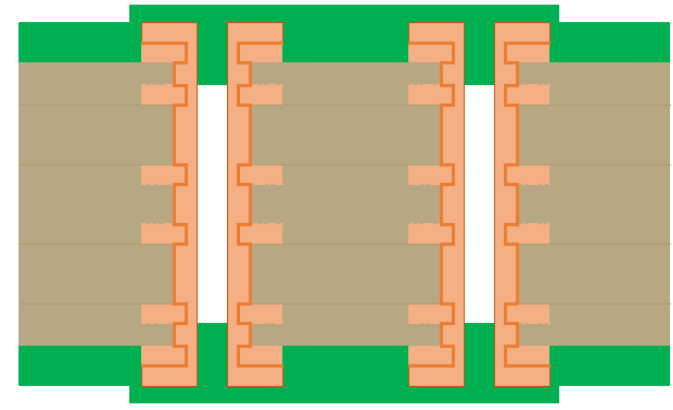




a. Solder mask

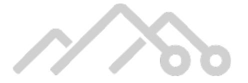


b. Solder mask with dry film tent

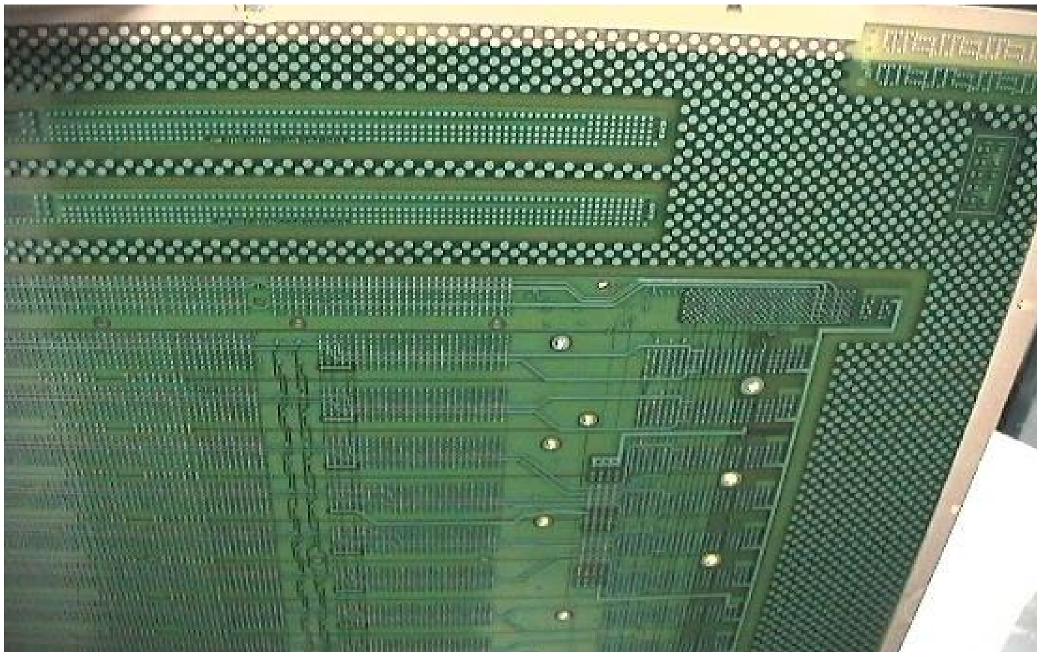


c. Solder mask plugging

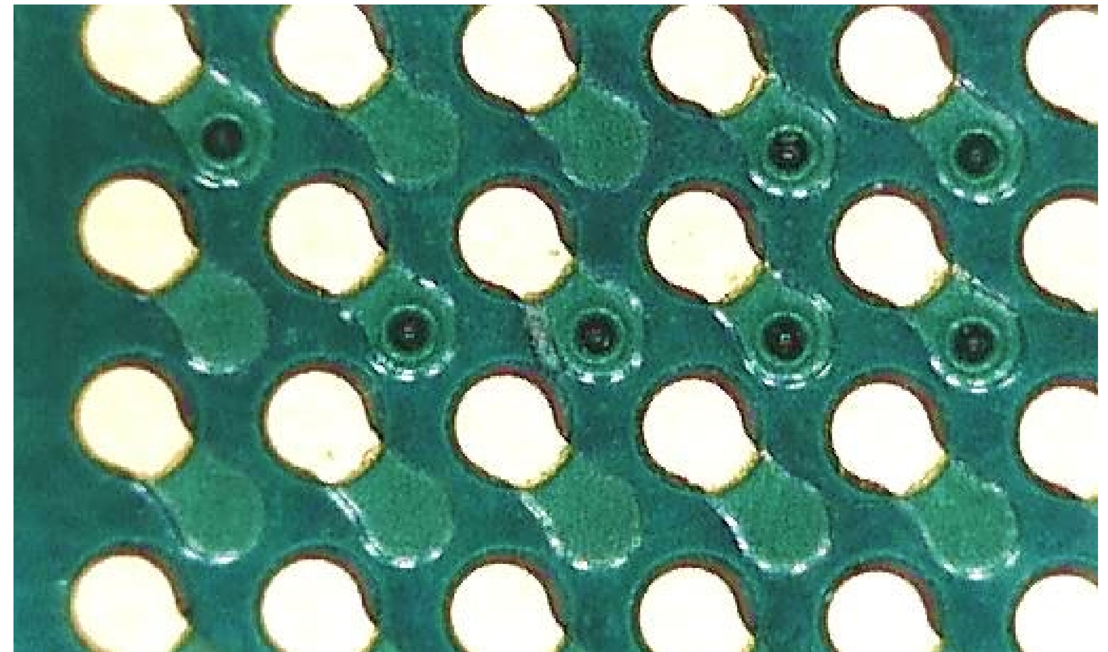
Solder Mask



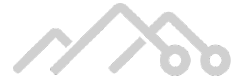
Panel coated with solder mask



Close-up of exposed copper and covered vias

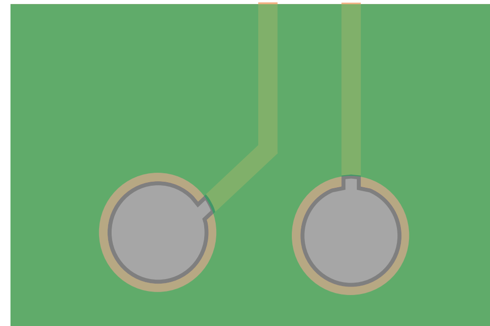


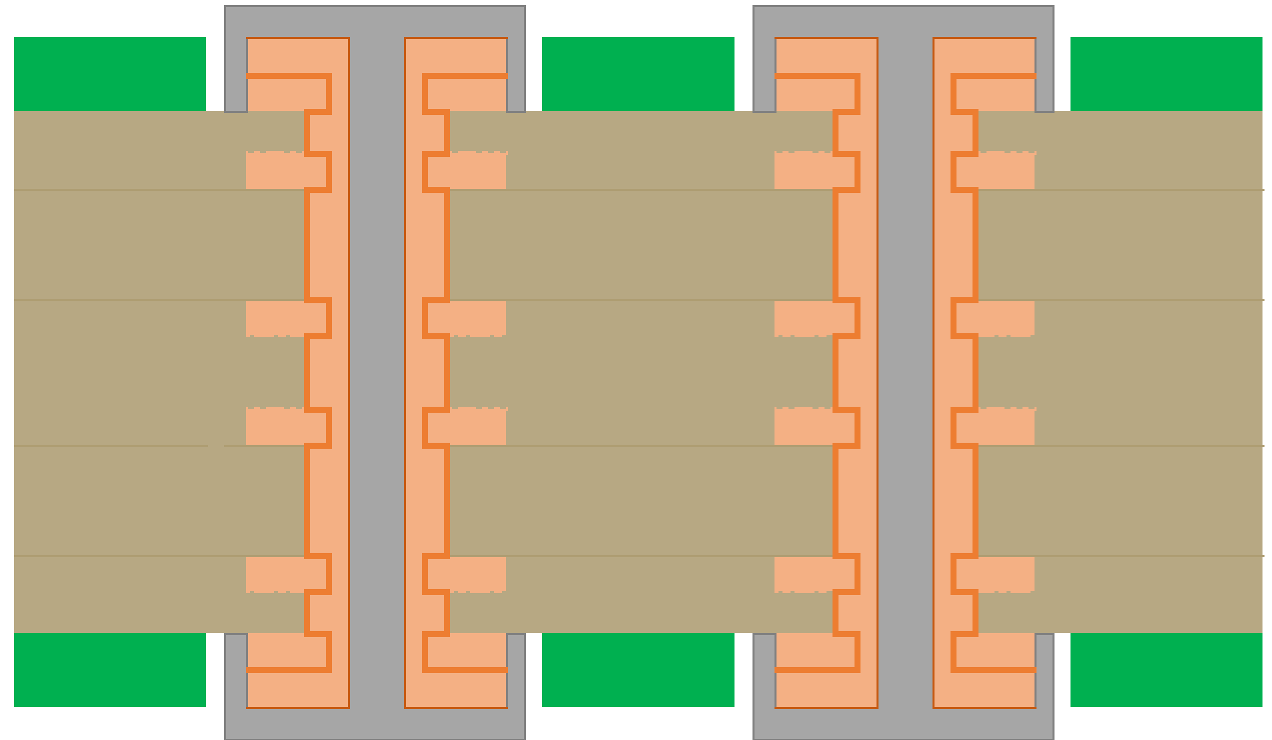
Step 15: Electrolytic Final Finish Plate



- Electroless Nickel, Immersion Gold (ENIG) is the most used final finish in North America
- Other common finishes are SnPb, HASL, ENEPIG, etc.

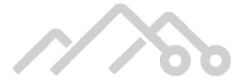
Final finish is applied to exposed copper to protect it from corrosion





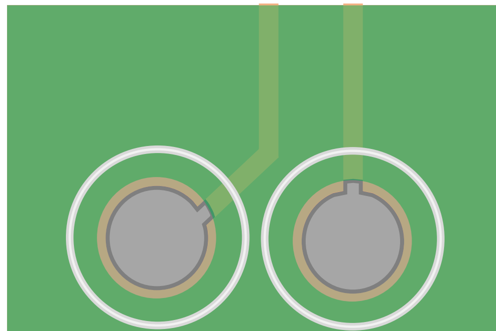
a. Final finish applied to exposed copper

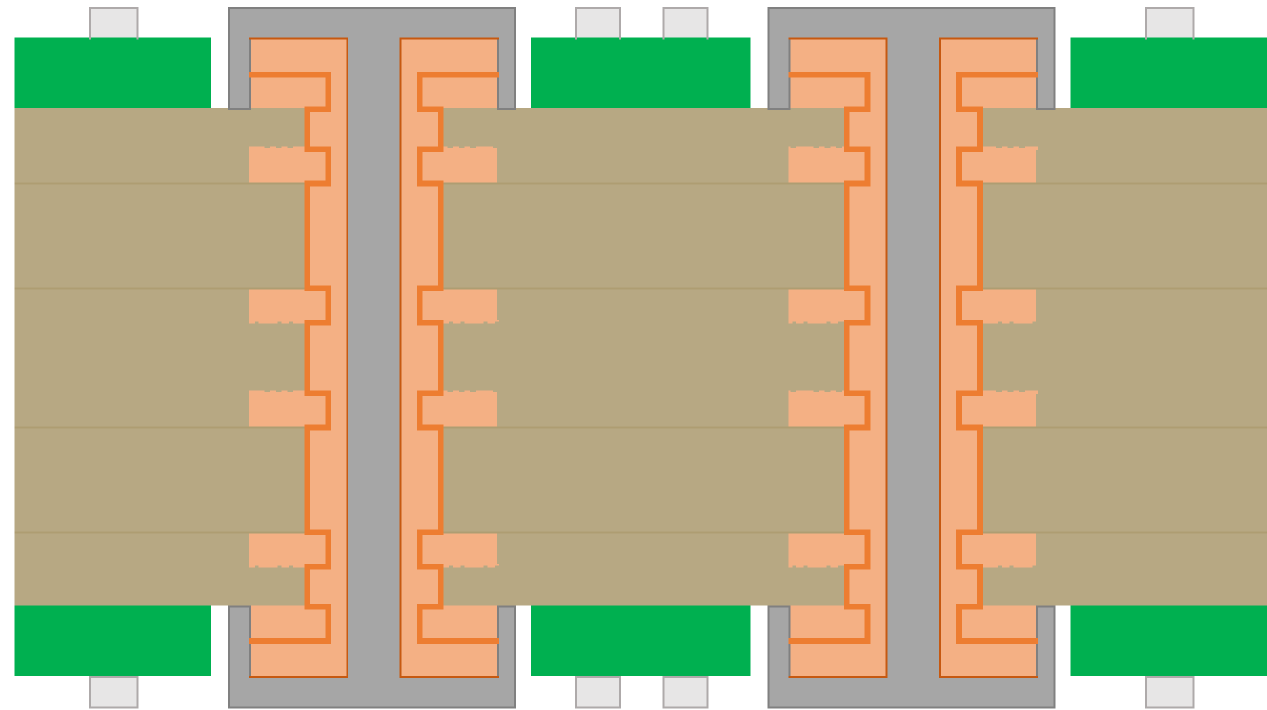
Step 16: Ink Legend



- The ink legend is often referred to as "silk screen" which is a term that originated from the prior way of "screening" legend onto boards

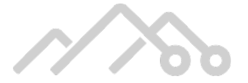
Legend is ink-jet printed over solder mask





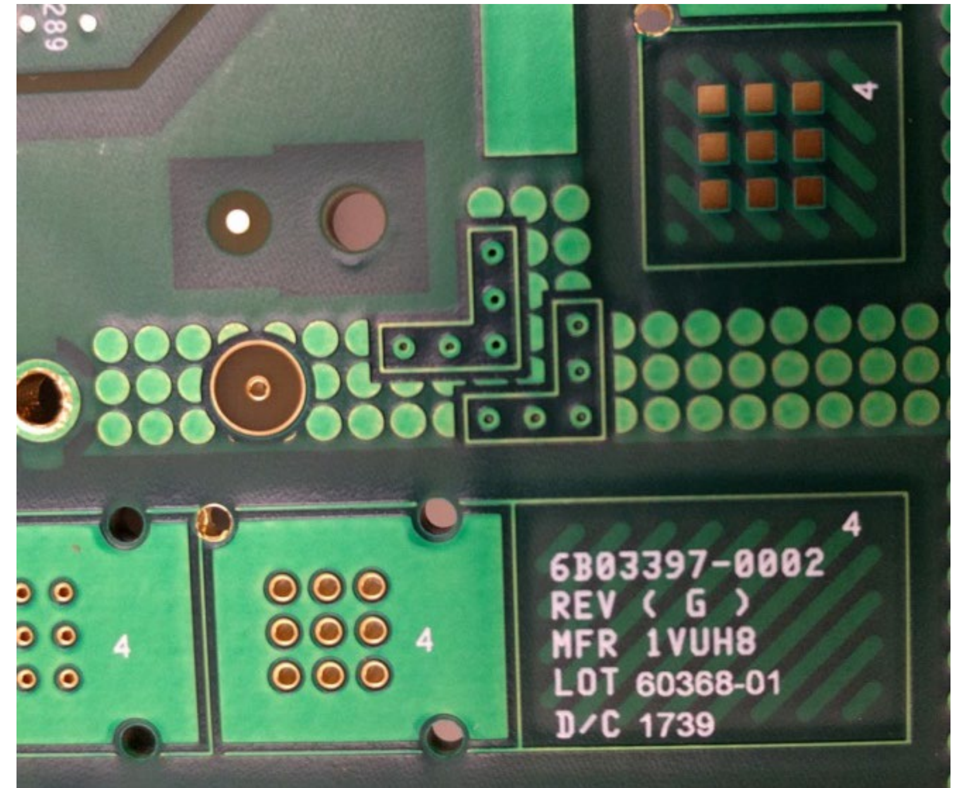
a. Ink legend applied over solder mask

Ink Legend Equipment

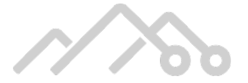


Ink Jet Printer

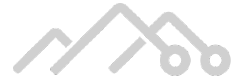
Legend



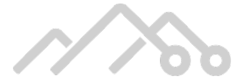
Step 17: Electrical Test



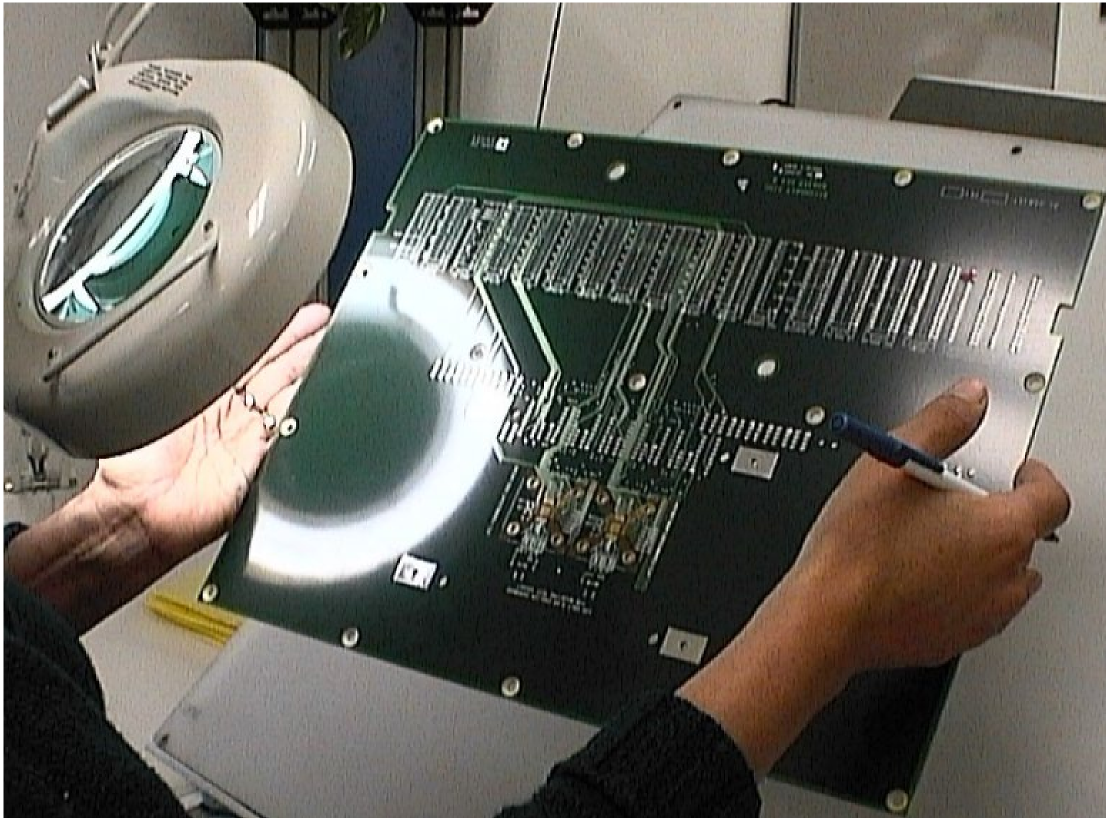
Step 18: Route Boards & Coupons



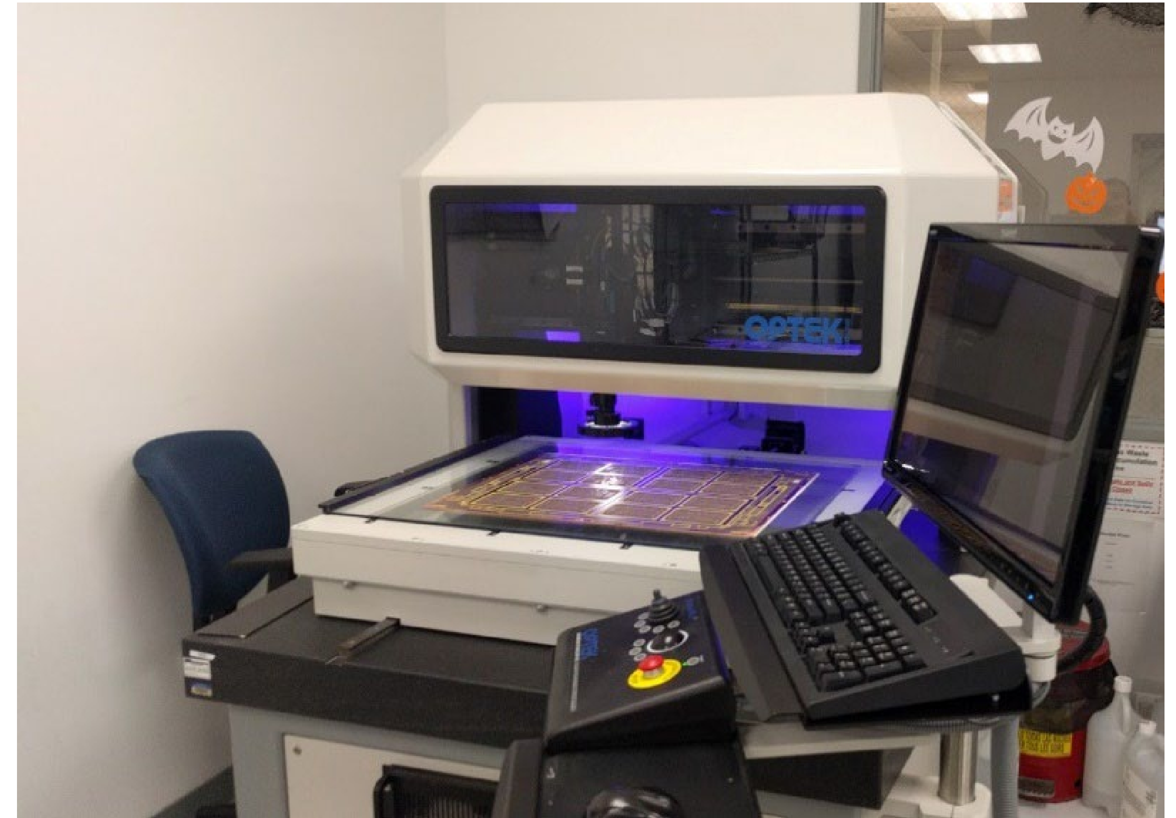
Step 19: Final Inspection



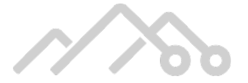
Final Inspection



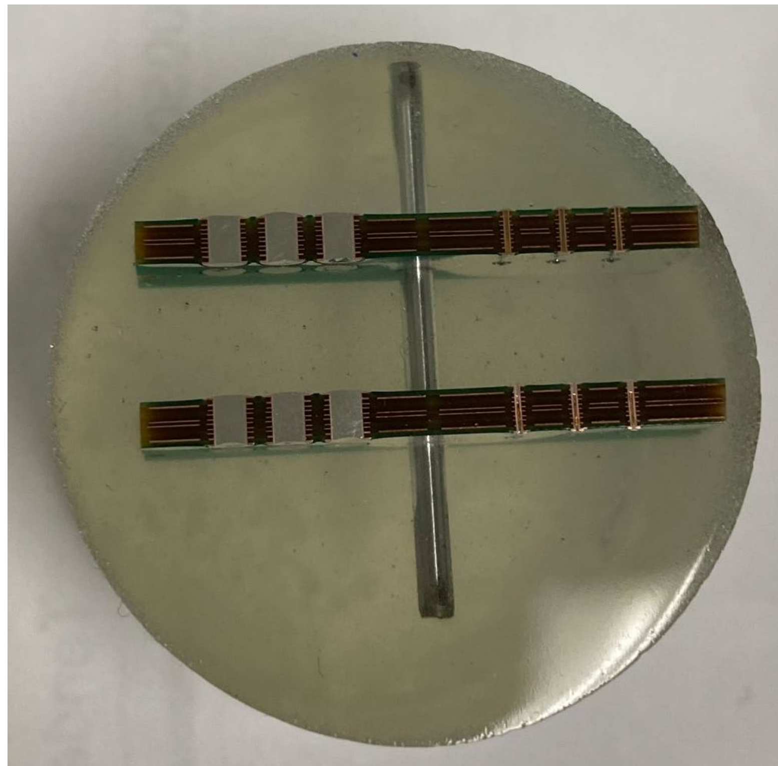
Coordinate Measuring Machine (CMM)



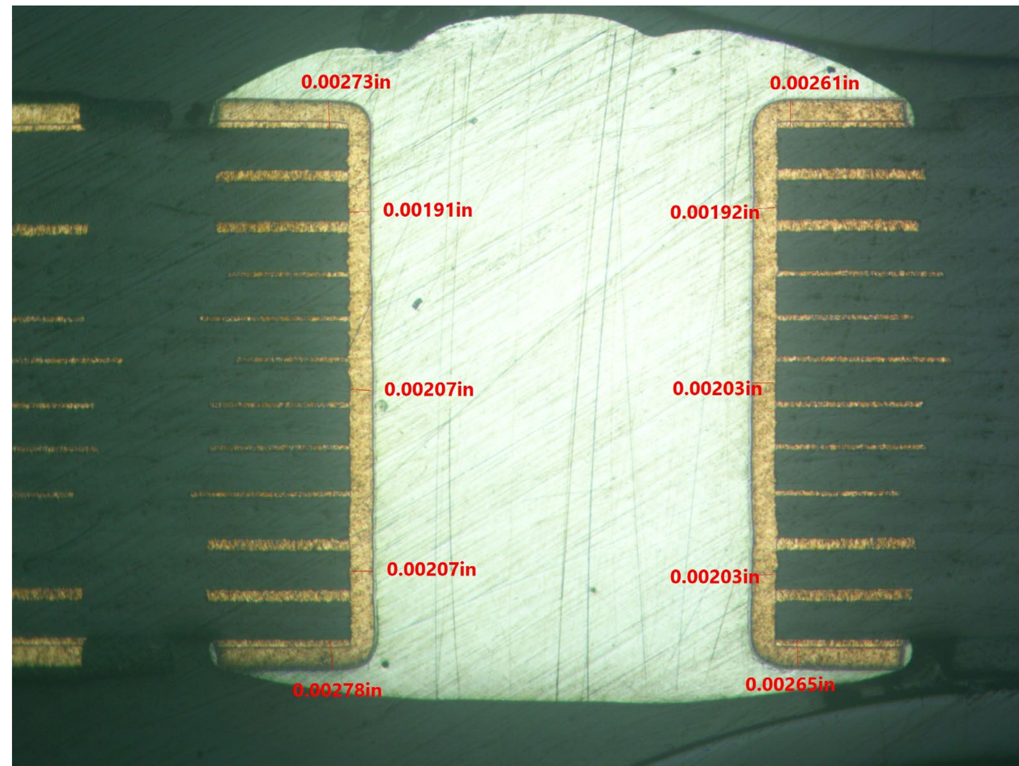
Step 20: Coupon Microsection & Analysis



Coupon Puck



Cross-section of coupon



Questions?